Please type a plus sign	(+) inside this box	+	
-------------------------	---------------------	---	--

PTO/SB/08A (08-00)

Approved for use through 10/31/2002. OMB 0651-0031 U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO	Complete if Kno

## INFORMATION DISCLOSURE STATEMENT BY APPLICANT

09/891,523 Application Number June 27, 2001 Filing Date RAKVIC et al First Named Inventor Technology Center 2100 Group Art Unit 2185

(use as many sheets as necessary)

TRADE TRADE

**Examiner Name** Not assigned 2207/1123601 of Attorney Docket Number

OCT 0 9 200 **U.S. PATENT DOCUMENTS** U.S. Patent Document Date of Publication of Pages, Columns, Lines, Where Relevant Name of Patentee or Applicant Cite No.1 Cited Document Passages or Relevant Kind Code<sup>2</sup> of Cited Document Number MM-DD-YYYY Figures Appear (if known) **FOREIGN PATENT DOCUMENTS** Foreign Patent Document Pages, Columns, Lines, Name of Patentee Date of Publication of Examiner Cite Where Relevant Cited Document or Applicant of Kind Code<sup>5</sup> Initials\* No.1 Passages or Relevant Office<sup>3</sup> Number<sup>4</sup> MM-DD-YYYY Cited Document T<sub>6</sub> (if known) Figures Appear

## OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Τ2	
MI		Agarwal et al, "Column-Associative Caches: A Technique for Reducing the Miss Rate of Direct-Mapped Caches", Proceedings, The 20 <sup>th</sup> Annual Intl Symposium on Computer Architecture, IEEE Computer Society, Technical Committee on Computer Architecture, Association for Computing Machinery SIGARCH, pp 169-190, San Diego, California, May 16-19, 1993		
MI		Alexander et al, "Distributed Prefetch-buffer/Cache Design for High Performance Memory Systems", Proceedings, Second Intl Symposium on High-Performance Computer Architecture, IEEE Computer Society, Technical Committee on Computer Architecture, pp 254-263, San Jose, California, February 3-7, 1996		
MI		Burger et al, "The SimpleScalar Tool Set, Version 2.0", Computer Sciences Department Technical Report, No. 1342, The University of Wisconsin, Madison, Wisconsin, June 1997		
MI		Edmondson et al, "Internal Organization of the Alpha 21164, a 300-MHz 64-bit Quad-issue CMOS RISC Microprocessor", <i>Digital Technical Journal</i> , Vol. 7, No. 1, pp 119-135, 1995		
MI		Hill, Mark D., "A Case for Direct-Mapped Caches", Computer, pp 25-40, December 1988		
MI		Juan et al, "The Difference-bit Cache", Proceedings, The 23 <sup>rd</sup> Annual Int'l Symposium on Computer Architecture, ACM SIGARCH, IEEE Computer Society, TCCA, pp 114-120, Philadelphia, Pennsylvania, May 22-24, 1996		
WI		Kessler et al, "Inexpensive Implementation of Set-Associativity", Proceedings, The 16 <sup>th</sup> Annual Intl Symposium on Computer Architecture, IEEE Computer Society Press, pp 131-139,1989		
Examiner Signature	\ \ \	1 Date Considered 6203	_]	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. Unique citation designation number.

Please type a plus show (+) inside this box

2185

Not assigned

2207/1123601

Approved for use through 10/31/2002. OMB 0651-0031

U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
in Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number. Substitute for form 1449A/PTO Complete if Known Application Number 09/891,523 **INFORMATION DISCLOSURE** June 27, 2001 Filing Date STATEMENT BY APPLICANT First Named Inventor RAKVIC et al

Group Art Unit

(use as many sheets as necessary)

**Examiner Name** of Sheet Attorney Docket Number

	<u> </u>	OTHER PRIOR ART NON PATENT LITERATURE DOCUMENTS	7
Examiner Initials *	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
MI		Rau et al, "Pseudo-Randomly Interleaved Memory", Proceedings, The 18 <sup>th</sup> Annual Intl Symposium on Computer Architecture, Association for Computing Machinery, pp 74-83, Toronto, Canada, May 27-30, 1991	
WI		Rivers et al, "On Effective Data Supply for Multi-Issue Processors", Proceedings, Intl Conference on Computer Design, VLSI in Computers and Processors, IEEE Computer Society Technical Committee on Design Automation, IEEE Circuits and Systems Society, pp 519-528, Austin, Texas, Oct. 12-15, 1997	
MI	:	Sánchez et al, "A Locality Sensitive Multi-Module Cache with Explicit Management", Proceedings of the 1999 Intl Conference on Supercomputing, ICS '99, Rhodes, Greece	
MI		Sohi et al, "High-Bandwidth Data Memory Systems for Superscalar Processors", ASPLOS-IV Proceedings, Fourth Intl Conference on Architectural Support for Programming Languages and Operating Systems, pp 53-62, Santa Clara, California, April 8-11, 1991	
WI		Wilson et al, "Increasing Cache Port Efficiency for Dynamic Superscalar Microprocessors", Proceedings, The 23 <sup>rd</sup> Annual Intl Symposium on Computer Architecture, ACM SIGARCH, IEEE Computer Society, TCCA, pp 147-157, Philadelphia, Pennsylvania, May 22-24, 1996	
MI		Wilson et al, "Designing High Bandwidth On-Chip Caches", "The 24 <sup>th</sup> Annual Intl Symposium on Computer Architecture, Conference Proceedings, ACM, pp 121-132, Denver, Colorado, June 2-4, 1997	
WI		Wilton et al, "An Enhanced Access and Cycle Time Model for On-Chip Caches", Digital WRL Research Report 93/5, Palo Alto, California, July 1994	

Examiner Signature	Midus Inoa	Date Considered	67	203	
			- 1		*